WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a substrate incorporating a semiconductor photodiode device having a p-n junction,

wherein the photodiode device includes at least one capacitive trench buried in the substrate and connected in parallel with the junction.

2. The integrated circuit according to claim 1,

wherein the substrate is formed from silicon, and

the capacitive trench includes an internal doped silicon region partially enveloped by an insulating wall that laterally separates the internal region from the substrate.

3. The integrated circuit according to claim 2, wherein the capacitive trench is surmounted by an upper doped silicon region, the upper region being in contact with the junction.

4. The integrated circuit according to claim 3,

wherein the substrate has a highly doped lower part with p-type conductivity and an upper part of p-type conductivity that is less doped than the lower part, and

the internal region and the upper region of the capacitive trench have n-type conductivity.

5. The integrated circuit according to claim 4, wherein the region of the junction having n-type conductivity includes a lower region of n-type conductivity that is in contact with the upper region of the trench, and an upper region of n-type conductivity that is more highly doped than the lower region.

6. A method for fabricating an integrated circuit including a substrate that incorporates a semiconductor photodiode device having a p-n junction, said method comprising the steps of:

producing an initial single-crystal substrate having locally a capacitive trench emerging at the surface of the initial substrate and forming a discontinuity in the crystal lattice;

recessing the initial substrate at the trench;

amorphizing the crystal lattice around the periphery of the recess;

depositing a layer of amorphous material having the same chemical composition as the initial substrate;

performing a thermal annealing in order to recrystallize the amorphous material so as to be continuous with the single-crystal lattice of the initial substrate; and

growing epitaxially an upper substrate layer.

7. The method according to claim 6, further comprising the step of planarizing the surface prior or subsequent to the step of performing the thermal annealing..

8. The method according to claim 7, wherein the step of planarizing the surface includes the sub-step of performing a chemical-mechanical polishing operation.

9. The method according to claim 6, wherein the step of amorphizing the crystal lattice includes the sub-step of performing a localized ion implantation around the recess through a masking operation.

10. The method according to claim 6, wherein the step of producing the initial substrate includes the sub-steps of:

depositing a first layer of a first material and a second layer of a second material in succession on the initial substrate;

etching a trench; and

filling the trench with a fill material, and

11. The method according to claim 10, wherein the step of recessing the initial substrate includes the sub-steps of:

selectively etching the first layer and an upper portion of the trench fill material with respect to the second layer so as to form lateral cavities and the recess at the crystal discontinuity; and

removing the second layer.

12. The method according to claim 11, wherein the sub-step of filling the trench includes:

lining the walls of the trench with oxide by thermal oxidation;

depositing highly doped polycrystalline silicon in the trench so as to fill it; and

etching the polycrystalline silicon so that the fill level of the trench is below the surface of the initial substrate.

13. The method according to claim 6, further comprising the step of forming the junction by n^+-type surface codiffusion of arsenic and phosphorus.

14. An information processing system including at least one integrated circuit, the integrated circuit comprising:

a substrate incorporating a semiconductor photodiode device having a p-n junction,

wherein the photodiode device includes at least one capacitive trench buried in the substrate and connected in parallel with the junction.

15. The information processing system according to claim 14,

wherein the substrate is formed from silicon, and

the capacitive trench includes an internal doped silicon region partially enveloped by an insulating wall that laterally separates the internal region from the substrate.

16. The information processing system according to claim 15, wherein the capacitive trench is surmounted by an upper doped silicon region, the upper region being in contact with the junction.

17. The information processing system according to claim 16,

wherein the substrate has a highly doped lower part with p-type conductivity and an upper part of p-type conductivity that is less doped than the lower part, and

the internal region and the upper region of the capacitive trench have n-type conductivity.

18. The information processing system according to claim 17, wherein the region of the junction having n-type conductivity includes a lower region of n-type conductivity that is in contact with the upper region of the trench, and an upper region of n-type conductivity that is more highly doped than the lower region.